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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/211,677	12/14/1998	HYUN CHANG LEE	8733D-7153	9588

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MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER
NGUYEN, KEVIN M

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/211,677	LEE, HYUN CHANG	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-36 and 51-55* is/are allowed.

6)☒ Claim(s) *37-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 1998* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 10/07/2002 is entered. The rejections of claims 37-50 are maintained.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the reference potential apply to the gate line signal and the reference potential is ground must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 37 and 50 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation "the reference potential is ground" is not properly described in the specification and the drawing as filed. Where a reference potential apply to the gate line signal. Where the reference potential is ground.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 38-41, 45-47 and 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Yasui et al (US 5,784,039).

As to claim 38, Yasui et al teach an active matrix liquid crystal display device having a plurality of pixels Lij (figure 1B), a source driver 2 connecting to n columns of source driver Si-Sn, and a gate driver 3 connecting to m+1 rows of gate buses Gi-Gm+1 (col. 4, lines 31-33);

the gate high voltage V_{GH} applies a first voltage to the gate signal line Gi. This voltage V_{GH} turns on the TFT for the data signal (Vs) applying to the pixel C_{LC} at the time period –to< t < t_1 (scanning clock signal) (the gate driver outputs the first voltage on a selected gate line during the application of a data signal in response to a scanning clock signal as claimed, figure 3A, col. 6, lines 1-45); the gate low voltage V_{GL} applied a

second voltage to the gate line Gi sequentially in response to a subsequent time period $t_1 < t < t_2$ (scanning clock signal) (the gate driver outputs the second voltage on the selected gate line during the application of the data signal in response to a subsequent scanning clock signal, wherein the second voltage is applied after the first voltage as claimed, figure 3B, col. 6, lines 46-58);

the gate high voltage V_{GH} applies a first voltage to the gate signal line Gi. This voltage V_{GH} turns on the TFT for the data signal (Vs) applying to the pixel C_{LC} at the time period $-to < t < t_1$ (each switching device having a gate electrode connected to the selected gate line applies the data signal to the pixel electrode in response to the first voltage as claimed, figure 3A, col. 6, lines 1-45);

the gate low voltage V_{GL} applied a second voltage to the gate line Gi sequentially. This voltage V_{GL} turns off the TFT for not connect the data signal (Vs) applying to the pixel C_{LC} at the time period $t_1 < t < t_2$ (each switching device having a gate electrode connected to the selected gate line turns off in response to the second voltage as claimed, figure 3B, col. 6, lines 46-58);

the gate low voltage V_{GL} is substantially equal to the potential (Vs) of the data signal so that could not turn on the TFT.

As to claim 39, Yasui et al teach the gate driver 3 sequentially changes the selected gate line Gi (see figure 7).

As to claim 40, Yasui et al teach the gate driver 3 includes a switch to select V_{GH} and V_{GL} (see figure 3A and figure 3B).

As to claim 41, Yasui et al teach figure 9 having a waveform V_{GH} and V_{GL} rise and fall times at leading and trailing edges of the gate pulse and the second bias voltage, respectively in Fig. 8A (the gate signal line potential drops from the V_{GH} to V_{GL} over a period of time t_6 to t_8, see figure 9, col. 4, lines 15-17).

As to claim 45, Yasui et al teach V_{GH} is greater than V_{GL} at period of time t_6 to t_9 (see figure 8A).

As to claim 46, Yasui et al teach the gate controller 3 inherently including the timing controller (t) (see figure 3).

As to claim 47, Yasui et al teach the gate controller 3 including the switches (SWi-1, SWi and SWi+1) being controlled by shift register (see figure 7).

As to claim 49, Yasui et al teach the first voltage V_{GH} being applied before the data signal (Vs) being applied (see figure 3A).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 42-44 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al in view Applicant's Admitted Prior Art hereinafter AAPA.

As to claims 42-44, Yasui et al teach all of the claimed limitation of claim 38, except for the gate signal line potential drops exponentially, linearly, and stepwise over the period of time. However, AAPA discloses that the scanning signal SCS changes in

the shape of the linear function as shown in Fig. 2A, an exponential function as shown in Fig. 2B, or a ramp function as shown in Fig. 2C (page 4, lines 17-20). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the scanning signal changing in the shape disclosed by AAPA in Yasui et al's TFT-LCD device because this would eliminate flickering and residual image (page 5, lines 29-30 of AAPA).

As to claim 48, AAPA discloses that the integrator 22 consists of a resistor R1 between the scanning driver cell 20 and the gate line GL, and a capacitor C1 connected between the gate line GL and the ground voltage line GVL (page 5, lines 2-5). Since a waveform modifying circuit such as an integrator for each gate line must be added (page 5, lines 30-32). Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the resistors and capacitors disclosed by AAPA in Yasui et al's TFT-LCD device because this would eliminate flickering and residual image (page 5, lines 29-30 of AAPA).

Allowable Subject Matter

9. Claims 27-36 and 51-55 allowed.

10. The following is a statement of reasons for the indication of allowable subject matter: Kobayashi et al (US 5,739,816) teach the reference voltage 7 is connected to the signal inverter circuit 9 (figure 1). Accordingly, the cited prior arts, alone or in combination, do not teach or fairly suggest "...the gate controller applies gate control signals that cause the gate driver to apply the reference potential to the gate signal line

after the application of the second signal voltage but during the application of the data signal on the data signal line..."

Response to Arguments

11. Applicant's arguments with respect to claims 37-50 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-FRI from 9:00-5:00 with alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Examiner
Art Unit 2674

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600